SHEET INDEX

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SYMBOL

SERIAL PERIPHERAL
INTERFACE A
CLEMENT IDENT.
A

TERM. MOC	FUNCT	TERM.	LOC
B000	I	004	2A9
B010	I	009	2A8
B020	I	105	2A7
B030	I	007	2A6
B040	I	309	2A6
B050	I	300	2A5
B060	I	107	2A5
B070	I	008	2A5
B080	I	014	2A3
B090	I	005	2A3
B100	I	201	2A2
B110	I	308	2A2
B120	I	003	2A1
B130	I	103	2A1
B140	I	102	2A1
B150	I	002	2A0
BPHO	I	104	2A0
BPLO	I	108	2A4
GINFO	I	106	2A4
GPO	I	202	3A6
GPRO	I	101	3A5
INTPO	I	302	3A4
RSHPOA	I	100	3A1
SPERI	I	006	2A9
BSDI	0	001	3G2
INF000	0	215	2G9
INF010	0	314	2G8
INF020	0	211	2G7
INF030	0	310	2G6
INF040	0	116	2G6
INF050	0	214	2G5
INF060	0	205	2G5
INF070	0	304	2G5
INF080	0	206	2G3
INF090	0	305	2G3
INF100	0	010	2G2
INF110	0	109	2G2
INF120	0	207	2G1
INF130	0	307	2G1
INF140	0	312	2G1
INF150	0	212	2G0
INFPHO	0	203	2G0
INFPLO	0	301	2G4
MYINTAN	0	219	3G5
MYINTAP	0	318	3G4
MYINTBN	0	218	3G6
MYINTBP	0	317	3G5
PTORO	0	019	3G1
RSET01	0	217	3G2
+5	P	000,019	3G6
GRD	G	200,319	3G6

RECORD OF CHANGES

DWG ISS	PREV FURN	STD	MFR DISC	SEE NOTE

SYSTEM USED ON	DESIGN CONTROL
COMMON SYSTEMS	IH

CURRENT DRAIN: 405mA

DWG ISSUE	EE OR CD ISSUED	DATE ISSUE	[illegible]	APPD
1	—	10-7-74	LAE LRE	RWF MTS RFG
2D1	—	12-8-75	P/S LRE	CE LEG RFG
3D1	—	7-20-77	TJW DKO	WJZ RKE JBD

NOTES:

1. ⏚ GROUND RETURN

2. UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN OHMS
CAPACITANCE VALUES ARE IN MICROFARADS
VALUES PRECEDED BY THE SYMBOL +(PLUS) OR -(MINUS) ARE IN VOLTS

3. BATTERY AND GROUND TERMINALS FOR INTEGRATED CIRCUITS

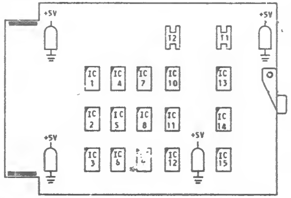
IC CODE	BAT. TERM	GRD TERM.
41BP	16	8
41CA	16	8
41CC	16	7,8
41DE	16	8

4. BATTERY AND GROUND TERMINALS FOR THIS CIRCUIT PACK ARE AS FOLLOWS:

FUNCTION	TERMINAL
+5	000,119
GRD	200,319

5. HORIZONTAL MOUNTING CENTERS AT 0.5 INCH.

6. INTEGRATED CIRCUIT AND TRANSFORMER LOCATION GUIDE:
(COMPONENT SIDE SHOWN)



UNMARKED COMPONENTS ARE FILTER CAPACITORS

SUPPORTING INFORMATION

CATEGORY	NO.
CIRCUIT PACK CODE	JK5
CONNECTOR ON FRAME	947C OR 947A
SERIES FOR LATEST CLASS A CHANGE. (ANY HIGHER SERIES IS ACCEPTABLE)	1
ACCEPTABLE SERIES	1

SHEET INDEX NOTES

1. WHEN CHANGES ARE MADE IN THIS DRAWING ONLY THOSE SHEETS AFFECTED WILL BE REISSUED.
2. THIS SHEET INDEX WILL BE REISSUED AND BROUGHT UP TO DATE EACH TIME ANY SHEET OF THE DRAWING IS REISSUED, OR A NEW SHEET IS ADDED.
3. THE ISSUE NUMBER ASSIGNED TO A CHANGED OR NEW SHEET WILL BE THE SAME ISSUE NUMBER AS THAT OF THE FIRST SHEET.
4. SHEETS THAT ARE NOT CHANGED WILL RETAIN THEIR EXISTING ISSUE NUMBER
5. THE LAST ISSUE NUMBER OF THE FIRST SHEET INDEX IS RECOGNIZED AS THE LATEST ISSUE NUMBER OF THE DRAWING AS A WHOLE.

NOTICE- NOT FOR USE OR DISCLOSURE OUTSIDE THE BELL SYSTEM EXCEPT UNDER WRITTEN AGREEMENT.

ISSUE
3D1

1N98

JK5 CIRCUIT PACK

SERIAL PERIPHERAL INTERFACE A
CIRCUIT

②

AT&TCO
STANDARD

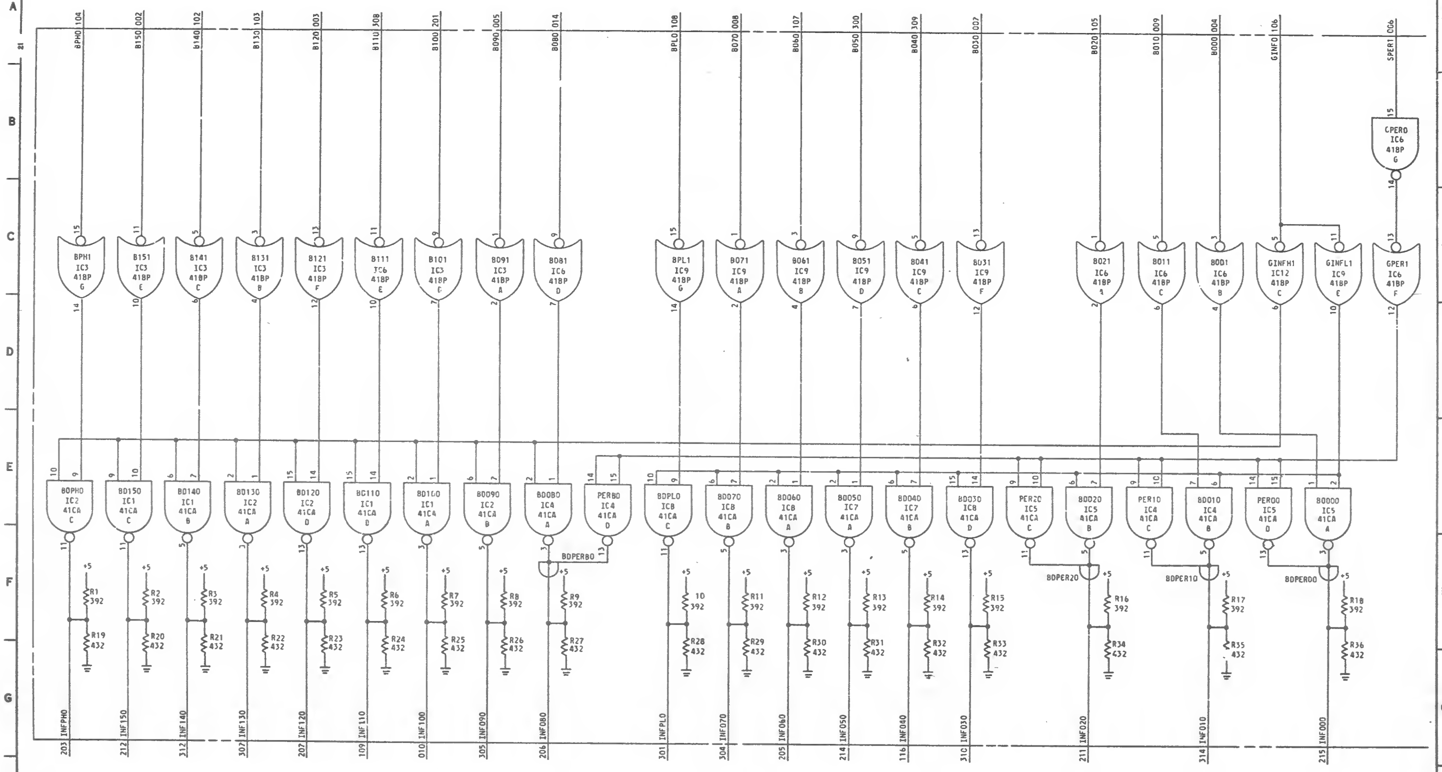
CPS-JK5
4 SHEETS

BELL TELEPHONE LABORATORIES
INCORPORATED

6S

PART OF CPS JK5

SERIAL PERIPHERAL INTERFACE A



CPS-JK5

ISSUE
1

JK5 CIRCUIT PACK

②

BELL TELEPHONE LABORATORIES
INCORPORATED

6S

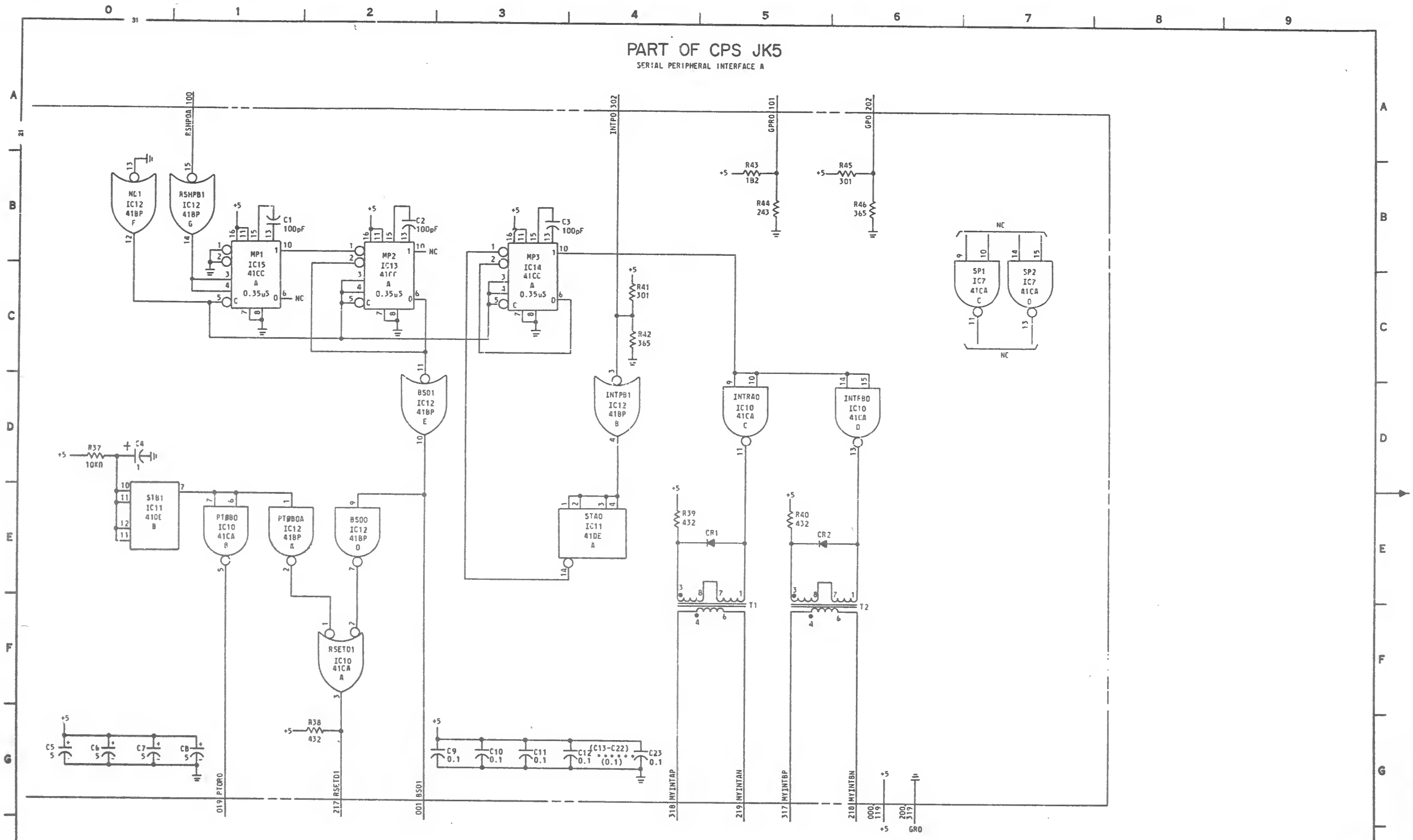
CPS-JK5

SHEET 2

PRINTED IN U. S. A.

PART OF CPS JK5

SERIAL PERIPHERAL INTERFACE A



CPS-JK5

ISSUE
1

JK5 CIRCUIT PACK ②

BELL TELEPHONE LABORATORIES

CPS-JK5

SHEET 3

PART OF CPS JK5

SERIAL PERIPHERAL INTEPFACE A

COMPONENT LIST

INTEGRATED CIRCUIT

LOC CODE ELEM	IC1 41CA		IC2 41CA		IC3 41BF		IC4 41CA		IC5 41CA		IC6 41BP	
ID	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC
A	BD100	2E2	BI130	2E1	B091	2C3	BD080	2E3	BD000	2E9	BD21	2C7
B	BD140	2E1	BDC90	2E3	B131	2C1	BD010	2EB	BD020	2E7	B001	2C8
C	BD150	2E0	BDPH0	2E0	B141	2C1	PER10	2E7	PER20	2E7	6D11	2C8
D	BD110	2E2	BD120	2E1	B101	2C2	PER80	2E4	PER00	2E8	B081	2C3
E					B151	2C0					B111	2C2
F					B121	2C1					GPER1	2C9
G					BPH1	2C0					GPERD	2B9

LOC CODE ELEM	IC7 41CA		IC8 41CA		IC9 41BP		IC10 41CA		IC11 41DE	
ID	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC
A	BD050	2E5	BD060	2E5	B071	2C5	RSETD1	3F2	STAD	3E4
B	BD040	2E6	BD070	2E4	B061	2C5	PTØBO	3E1	STB1	3E0
C	SP1	3C7	BDPL0	2E4	B041	2C6	INTRAD	3D5		
D	SP2	3C7	BD030	2E6	B051	2C5	INTRBD	3D6		
E					GINFL1	2C9				
F					BD31	2C6				
G					BPL1	2C4				

LOC CODE ELEM	IC12 41BP		IC13 41CC		IC14 41CC		IC15 41CC	
ID	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC
A	PTØBOA	3E1	MP2	3C2	MP3	3C3	MP1	3C1
B	INTPB1	3D4						
C	GINFH1	2C8						
D	BSDG	3E2						
E	BSD1	3D2						
F	HD1	3B0						
G	RSHPB1	3B1						

CAPACITOR

DESIG	CODE
C1-C3	~~KS-18250 L22~~,100PF KS-20676 L3
C4	600A,1
C5-C8	601A,5
C9-C23	KS-19774 L5,0.1

DIODE

DESIG	CODE
CR1,CR2	458C

RESISTOR

DESIG	CODE
R1-R18	KS-20616 L1A,392
R19-R36	,432
R37	,10KΩ
R38-R40	,432
R41	,301
R42	,365
R43	,182
R44	,243
R45	,301
R46	KS-20616 L1A,365

TRANSFORMER

DESIG	CODE
[2] T1,T2	2664G

CIRCUIT DESCRIPTION:

THIS CIRCUIT PACK CONTAINS 18 BUFFER RECEIVERS AND 18 OPEN COLLECTOR BUS DRIVERS FOR THE 18 INFORMATION LEADS. TRANSMISSION LINE TERMINATIONS ARE PROVIDED BY RESISTIVE VOLTAGE DIVIDERS FOR EACH OF THE INFORMATION LEADS. LEAD GINFD BEING LOW GATES THE BUS DRIVERS ON.

LEAD SPER1 BEING HIGH GATES LEADS INFO00, INFO10, INFO20, AND INFO80 TO GROUND LEVEL. THIS BIT CONFIGURATION IS THE PARITY ERROR REPLY MESSAGE.

THE 50% DUTY CYCLE PULSE TRAIN ON LEAD RSHPOA DRIVES THE RETRIGGERABLE MONOPULSER MP1. THE LEADING EDGE OF THE FIRST PULSE SETS THE "1" OUTPUT OF MP1 HIGH. WHEN THE INCOMING PULSE TRAIN IS INTERRUPTED BY ABOUT 350 NSEC THE OUTPUT OF MP1 RETURNS TO GROUND LEVEL. THIS GROUND GOING TRANSITION TRIGGERS MP2 TO GENERATE A 350 NSEC WIDE RESET PULSE ON LEADS BSO1 AND RSETO1.

TWO CABLE DRIVERS CAN BE USED TO TRANSMIT DEMAND INTERRUPT PULSES TO BOTH CC'S. THESE PULSES ARE GENERATED BY HIGH TO LOW TRANSITIONS ON LEAD INTPO.

THE RC NETWORK (R37,C4) AT THE INPUT OF SCHMITT TRIGGER STB1 CREATES AN EXPONENTIAL VOLTAGE RISE AS THE +5V POWER IS APPLIED TO THE CIRCUIT. AS LONG AS THE CAPACITOR VOLTAGE IS BELOW THE INPUT THRESHOLD LEVEL OF STB1, THE OUTPUT OF STB1 IS HIGH. THIS HIGH LEVEL KEEPS THE RSETO1 LINE ACTIVE. THE SPI CONTROL LOGIC IS INITIALIZED BY THIS HIGH LEVEL.

ISSUE 3D1

JKS CIRCUIT PACK ②

BELL TELEPHONE LABORATORIES
INCORPORATED

6S

CPS-JK5
SHEET 4

CPS-JK5